

### **LISTING OF CLAIMS**

The following listing of claims will replace all prior versions, and listings, of claims in the application.

5           1.       (Currently Amended) A sense amplifier, comprising:

an input stage having a pair of balanced isolation devices, each of the pair of balanced isolation devices having an input connected to receive a separate one of a pair of differential input signals, each of the pair of balanced isolation devices having a gate connected to receive a common bias voltage; and

10           a sense stage having a pair of sense nodes connected to receive respective output signals from the pair of balanced isolation devices of the input stage, the sense stage being further configured to amplify a voltage of the received output signal having the higher voltage, wherein the sense stage includes a pair of booster circuits, each of the pair of booster circuits being configured to assist in a low-to-high state transition of a separate  
15       one of the pair of sense nodes during a sensing operation,

wherein each of the pair of booster circuits includes,

a NAND device connected to receive an equalization control signal as a first input and a state of the sense node to which the booster circuit is connected as a second input,

a PMOS device having an input connected to a supply voltage and an output  
20 connected to the sense node to which the booster circuit is connected, the PMOS device having a gate connected to receive an output of the NAND device.

2. (Original) A sense amplifier as recited in claim 1, wherein the gates of the pair of balanced isolation devices are connected together to receive the common bias voltage.

5 3. (Original) A sense amplifier as recited in claim 1, wherein each of the pair of balanced isolation devices is defined as a PMOS device.

4. (Original) A sense amplifier as recited in claim 1, wherein the common bias voltage is provided by a bias generator circuit.

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5. (Original) A sense amplifier as recited in claim 1, wherein the common bias voltage is maintain at a level that is about one-half of a supply voltage level.

15 6. (Previously Presented) A sense amplifier as recited in claim 1, wherein each of the pair of sense nodes is connected to an output of a separate one of the pair of balanced isolation devices of the input stage.

7. (Previously Presented) A sense amplifier as recited in claim 1,  
20 wherein the sense stage includes a transmission gate disposed between the pair of sense nodes, the transmission gate being configured to control electrical conduction between the pair of sense nodes, the transmission gate being further configured to operate in response to an equalization control signal.

25 8. (Cancelled)

9. (Currently Amended) A sense amplifier, comprising:

a pair of input nodes connected to each receive a separate one of a pair of differential input signals;

5 a pair of balanced isolation devices each having an input connected to a separate one of the pair of input nodes, the pair of balanced isolation devices each having a gate connected to receive a common bias voltage, the pair of balanced isolation devices each having an output representing a separate one of a pair of sense nodes;

10 a transmission gate disposed between the pair of sense nodes, the transmission gate being configured to control conduction between the pair of sense nodes;

pull down logic being connected to the pair of sense nodes; ~~and~~

a pair of booster devices configured to assist a low-to-high state transition of a respective one of the pair of sense nodes during a sensing operation; and

15 a recovery stage configured to assist charging and equalizing the pair of input nodes prior to activating the sense amplifier to perform a sensing operation.

10. (Original) A sense amplifier as recited in claim 9, wherein each of the pair of balanced isolation devices is a PMOS device.

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11. (Original) A sense amplifier as recited in claim 9, wherein the transmission gate includes a PMOS device having a first terminal connected to one of the pair of sense nodes and a second terminal connected to the other of the pair of sense nodes, the transmission gate PMOS device having a gate connected to receive an equalization control signal.

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12. (Cancelled)

13. (Previously Presented) A sense amplifier as recited in claim 9,  
5 wherein each of the pair of booster devices includes,

a NAND device connected to receive an equalization control signal as a first input  
and a state of the sense node to which the booster device is connected as a second input,

a PMOS device having an input connected to a supply voltage and an output  
connected to the sense node to which the booster device is connected, the PMOS device  
10 having a gate connected to receive an output of the NAND device,

wherein receipt of a low equalization control signal causes the output of the  
NAND device to maintain a high state such that the PMOS device is controlled to not  
transmit, receipt of a high equalization control signal causing the output of the NAND  
device to attain a state opposite from a state of the sense node to which the booster device  
15 is connected.

14-15. (Cancelled)

16. (Original) A sense amplifier as recited in claim 9, further comprising:  
20 a bias generator configured to supply the common bias voltage to the gates of the  
pair of balanced isolation devices.

17. (Original) A sense amplifier as recited in claim 16, wherein the bias  
generator is configured to maintain the common bias voltage at about one-half of a supply  
25 voltage level.

18. (Cancelled)

19. (Original) A sense amplifier as recited in claim 9, wherein the pull  
5 down logic includes a pair of NMOS devices each having an input connected to a  
separate one of the pair of sense nodes, each of the pair of NMOS devices having a gate  
connected to the input of the other one of the pair of NMOS devices, each of the pair of  
NMOS devices having an output connected to ground.

10 20. (Currently Amended) A method for making a sense amplifier, comprising:  
connecting a pair of input nodes to each receive a separate one of a pair of  
differential input signals;

connecting an input of each of a pair of balanced isolation devices to a separate  
one of the pair of input nodes, wherein each of the pair of balanced isolation devices has  
15 an output representing a separate one of a pair of sense nodes;

connecting a gate of each of the pair of balanced isolation devices to receive a  
common bias voltage;

connecting each of a first terminal and a second terminal of a transmission gate to  
a separate one of the pair of sense nodes;

20 connecting pull down circuitry to the pair of sense nodes; ~~and~~

connecting each of a pair of booster devices to a separate one of the pair of sense  
nodes, each of the pair of booster devices being configured to assist a low-to-high state  
transition of the sense node to which the booster device is connected during a sensing  
operation; and

connecting a recovery stage to the pair of input nodes, wherein the recovery stage is defined to assist in charging and equalizing the pair of input nodes prior to activating the sense amplifier to perform a sensing operation.

5           21.   (Original)    A method for making a sense amplifier as recited in claim 20, wherein each of the pair of balanced isolation devices is defined as a PMOS device.

          22.   (Original)    A method for making a sense amplifier as recited in claim 20, wherein the transmission gate is defined as a PMOS device.

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          23.   (Original)    A method for making a sense amplifier as recited in claim 22, further comprising:

          connecting a gate of the PMOS device of the transmission gate to receive an equalization control signal.

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          24.   (Cancelled)

          25.   (Previously Presented)    A method for making a sense amplifier as recited in claim 20, wherein connecting each of the pair of booster devices to the separate one of the pair of sense nodes includes,

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          connecting a first input of a NAND device to receive an equalization control signal,

          connecting a second input of the NAND device to receive a state of the sense node to which the booster device is connected,

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          connecting an input of a PMOS device to a supply voltage,

connecting an output of the PMOS device to the sense node to which the booster device is connected, and

connecting a gate of the PMOS device to receive an output of the NAND device.

5           26.     (Previously Presented)     A method for making a sense amplifier as recited in claim 20, further comprising:

connecting an output of each of a pair of PMOS devices to a separate one of the pair of input nodes;

connecting an input of each of the pair of PMOS devices to a supply voltage; and

10           connecting a gate of each of the pair of PMOS devices to a ground.

27.     (Original)     A method for making a sense amplifier as recited in claim 20, further comprising:

15           connecting a bias generator to supply the common bias voltage to the gates of the pair of balanced isolation devices, wherein the bias generator is defined to maintain the common bias voltage at about one-half of a supply voltage level.

28.     (Cancelled)

20           29.     (Original)     A method for making a sense amplifier as recited in claim 20, wherein connecting pull down circuitry to the pair of sense nodes includes,

connecting an input of each of a pair of NMOS devices to a separate one of the pair of sense nodes,

connecting an output of each of the pair of NMOS devices to a ground, and

connecting a gate of each of the pair of NMOS devices to the input of the other one of the pair of NMOS devices.